CLAIMS

WHAT IS CLAIMED:

1. A method for determining critical timing path sensitivities of macros in a semiconductor device, comprising:

configuring a timing parameter of a particular macro in the semiconductor device;

determining a first maximum operating frequency of the semiconductor device configured in accordance with the timing parameter;

changing the timing parameter of the particular macro;

determining a second maximum operating frequency of the semiconductor device configured in accordance with the changed timing parameter; and

determining a contribution of the selected macro to a critical timing path of the semiconductor device based on the first and second maximum operating frequencies.

2. The method of claim 1, wherein configuring the timing parameter further comprises configuring a self-timed pulse control (STPC) parameter of the selected macro.

3. The method of claim 2, wherein changing the timing parameter further comprises decreasing the STPC parameter.

4. The method of claim 3, wherein determining the contribution of the selected macro to the critical timing path of the semiconductor device further comprises determining that the selected macro has a positive effect on the critical timing path in response to the second maximum operating frequency being greater than the first maximum operating frequency.

5. The method of claim 2, wherein changing the timing parameter further comprises increasing the STPC parameter.

6. The method of claim 5, wherein determining the contribution of the selected macro to the critical timing path of the semiconductor device further comprises determining that the selected macro has a positive effect on the critical timing path in response to the second maximum operating frequency being less than the first maximum operating frequency.

7. The method of claim 1, wherein determining the contribution of the selected macro to the critical timing path of the semiconductor device further comprises determining that the selected macro has a limited effect on the critical timing path in response to the second maximum operating frequency being substantially the same as the first maximum operating frequency.

8. The method of claim 1, further comprising changing a default STPC setting of the selected macro based on the first and second maximum operating frequencies.

9. A system for testing a semiconductor device including a plurality of macros, comprising:

a tester adapted to configure a timing parameter of a particular macro in the semiconductor device, determine a first maximum operating frequency of the semiconductor device configured in accordance with the timing parameter, change the timing parameter of the particular macro, and determine a second

maximum operating frequency of the semiconductor device configured in accordance with the changed timing parameter; and

a controller adapted to receive the first and second maximum operating frequencies and determine a contribution of the selected macro to a critical timing path of the semiconductor device based on the first and second maximum operating frequencies.

10. The system of claim 9, wherein the timing parameter further comprises a self-timed pulse control (STPC) parameter of the selected macro.

11. The system of claim 10, wherein the tester is adapted to decrease the STPC parameter.

12. The system of claim 11, wherein the controller is adapted to indicate that the selected macro has a positive effect on the critical timing path in response to the second maximum operating frequency being greater than the first maximum operating frequency.

13. The system of claim 10, wherein the tester is adapted to increase the STPC parameter.

14. The system of claim 13, wherein the controller is adapted to indicate that the selected macro has a positive effect on the critical timing path in response to the second maximum operating frequency being less than the first maximum operating frequency.

15. The system of claim 9, wherein the controller is adapted to indicate that the selected macro has a reduced effect on the critical timing path in response to the second maximum operating frequency being substantially the same as the first maximum operating frequency.

16. A system for determining critical timing path sensitivities of macros in a semiconductor device, comprising:

means for configuring a timing parameter of a particular macro in the semiconductor device;

means for determining a first maximum operating frequency of the semiconductor device configured in accordance with the timing parameter;

means for changing the timing parameter of the particular macro;

means for determining a second maximum operating frequency of the semiconductor device configured in accordance with the changed timing parameter; and

means for determining a contribution of the selected macro to a critical timing path of the semiconductor device based on the first and second maximum operating frequencies.